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NEW METHODOLOGY TO MEASURE MANY MORE TRANSISTORS ON THE SAME TEST AREA

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Background

The present invention generally relates to methodologies for measuring transistors, and more specifically relates to a new methodology for measuring many more transistors on a given test area than a conventional methodology provides.

A conventional method to measure a transistor matrix is illustrated in Figure 1. As shown, the methodology provides that a pad group 10 is used (as an example, Figure 1 illustrates a 2 x 10 pad group). In the methodology, test structuires 12 (i.e., transistors) are placed in empty spaces between the pads 14. Using a shared gate and source, one 2 x 10 pad group can hold up to 9 test structures (i.e., transistors).

One drawback of this methodology is the effective usable area for transistor measurement is very small compared to the total test structure area. For example, in the 2 x 10 pad group as illustrated in Figure 1, the effective transistor area is only up to 0.6% of the total test structure area.

Objects and Summary

An object of an embodiment of the present invention is to provide a test methodology which allows for more efficient use of a given test structure area.

Another object of an embodiment of the present invention is to provide a test methodology which provides that effective transistor area is increased with regard to a given test structure area.

Still another object of an embodiment of the present invention is to provide a test methodology which uses a test area much more efficiently.

Briefly, and in accordance with at least one of the foregoing objects, an embodiment of the present invention provides a system for testing test structures. The system provides that the test structures, such as transistors, are arranged in a plurality of test array rows. A logic circuit controls which test structures are to be measured (i.e., which row of test structures is to be measured).

Specifically, preferably an incrementer is configured to receive a triggering signal, and the incrementer is configured to function as an address adder. More specifically, preferably the incrementer is configured such that each time the triggering signal rises from 0 to 1 the output of the incrementer increases by 1 (i.e., a different sequence of output lines becomes active). Preferably, the output of the incrementer serves as the address input into a decoder, and the decoder is connected to the rows of test structures and is configured to activate one row at a time. Preferably, each test structure contains a control circuit which is controlled by this signal (i.e., the output of the decoder). If the test structures are transistors, bias to each of the transistors can be applied separately with a common gate,

source and well, and measurement can be done with a separate drain node.

Brief Description of the Drawings

The organization and manner of the structure and operation of the invention, together with further objects and advantages thereof, may best be understood by reference to the following description, taken in connection with the accompanying drawing, wherein:

Figure 1 illustrates use of a 2 x 10 pad group in a conventional transistor measurement methodology;

Figure 2 illustrates a system that includes an incrementer and decoder and is configured for testing test structures pursuant to a methodology which is in accordance with an embodiment of the present invention;

Figure 3 provides an input-output table of the incrementer illustrated in Figure 2;

Figure 4 provides an input table of the decoder illustrated in Figure 2; and

Figure 5 illustrates a test structure which can be used in association with the system illustrated in Figure 2.

Description

While the invention may be susceptible to embodiment in different forms, there is shown in the drawings, and herein will be described in detail, a specific embodiment with the understanding that the present disclosure is to be considered an exemplification of the principles of the invention, and is not intended to limit the invention to that as illustrated and described herein.

Figure 2 illustrates a system 20 for testing test structures 22. The system 20 provides that the test structures 22, such as transistors, are arranged in a plurality of test array rows (represented by dots 24 in Figure 2). The system includes a logic circuit 26 which controls which row of test structures is to be measured. The logic circuit 26 includes an incrementer 28 and decoder 30. The incrementor 28 is configured to receive a triggering signal 32 through an input 34 and function as an address adder. More specifically, preferably the incrementer 28 is configured such that each time the triggering signal 32 rises from 0 to 1, the output 36 of the incrementer 28 increases by 1 (i.e., a different sequence of output lines 38 becomes active). Figure 3 provides an input-output table of the incrementer 28, wherein the incrementer 28 has eight output lines 38 providing 256 possible output line sequence combinations.

Preferably, the output 36 of the incrementer 28 serves as the address input 38 into the decoder 30, and the decoder 30 is connected to the rows of test structures and is configured to activate one row at a time. Figure 4 provides an input table of the decoder, where the decoder has eight address inputs providing 256 possible input line sequence combinations. In such case, it would be assumed

that 256 rows of test structures would be connected to the output lines 40 of the decoder 30. In Figure 4, the input sequence which is shown in the first (i.e., left-most in the table) column 42 would provide that only the first row of test structures is on (i.e., measured), the input sequence which is shown in the second column 44 would provide that only the second row of test structures is on (i.e., measured), the input sequence which is shown in the third column 46 would provide that only the third row of test structures is on (i.e., measured), . . . the input sequence which is shown in the 256^{th} column 48 would provide that only the 256^{th} row of test structures is on (i.e., measured). When the decoder 30 is reset, none of the rows of test structures are on.

Figure 5 illustrates an exemplary test structure 22. As shown, preferably each test structure 22 includes a Device under test (DUT) 80, i.e., a transistor, and a control circuit 82. As shown, the control circuit 82 may consist of pass gates, specifically an N-channel pass gate transistor 84 and a P-channel pass gate transistor 86 to pass over the gate voltage 88, an input control 89, and an inverter 90 to supply the pMOS pass gate 86. If the DUT 80 is a transistor, bias to each of the transistors can be applied separately with a common gate 92, source 94 and well 96, and measurement can be done with a separate drain node (identified with reference numeral 52 in Figures 2 and 5).

If sixteen test structures are arranged in each row, by activating one row, 16 devices can be measured simultaneously. If eight address lines into the decoder 30 are used, and each triggering signal increments one address consecutively (see the table illustrated in Figure 3), there are 256 total possible address outputs which can

be generated by the incrementer 28. From these 256 addresses, the decoder will incrementally activate 256 different rows in the test array (see the table illustrated in Figure 4). If the test structures are arranged in 256 rows and 16 columns, 4096 transistors can be measured from this test array. To measure 4096 transistors, 256 triggering signals are needed. Of course, the less transistors desired to be measured, the less times the input signal into the incrementor needs to be triggered.

Assuming 10x5um^2 is needed for each test structure, and 512 transistors need to be measured, 32 rows and 16 columns of test structures would be needed, with a total test area of 0.0256 mm^2. With one 2x10 pad group (240x1200um^2), 16 pads would be used for drain outputs, one common gate, one common well, one common source, and one trigger signal. Two pad groups would be sufficient to measure the 512 transistors, a big savings compared to using 30 pad groups to measure the 512 transistors, with a total area of 8mm^2.

The present invention provides a test methodology which allows for more efficient use of a given test structure area, provides that effective transistor area is increased with regard to a given test structure area, and that a test area is used much more efficiently than the conventional, widely used methodology.

While an embodiment of the present invention is shown and described, it is envisioned that those skilled in the art may devise various modifications of the present invention without departing from the spirit and scope of the appended claims. For example, while Figures 3 and 4 relate to the situction wherein the incrementor has eight output lines and the decoder has eight address inputs and 256 output lines, this is not imperative, and other sized incrementors and decoders

can be used. In fact, while Figure 2 illustrates a logic circuit which includes an incrementer and decoder, other types of logic circuits can be employed in practicing the present invention.